Please cancel Claims 1-17 and add new Claims 18-22 as shown in this complete set of all pending Claims:

1 – 17 (Cancelled)

18. (New) A data processing system, comprising:

a non-volatile memory unit having an address input, a data input and a corrected data output, the non-volatile memory unit comprising:

a main memory coupled to the data input and the address input for storing signal groups;

an error checking and correction (ECC) memory coupled to the data input and the address input for storing error correction bits, wherein the main memory and the ECC memory determine a first logic state by means of a stored charge and determine a second logic state by means of a lack of stored charge;

error checking and correction (ECC) circuitry coupled to the main memory and to the ECC memory being operable to detect an error in a signal group retrieved from the main memory in response to an address provided on the address input, and being operable to correct the error in the signal group and to output the corrected signal group on the corrected data output, the ECC circuitry comprising:

interrupt circuitry operable to selectively signal an interrupt, such that an interrupt is signaled when the ECC circuitry determines the error in the signal group resulted from a bit signal that should be in the first state but was instead in the second state, and such that an interrupt is not signaled when the ECC circuitry determines the error in the signal group resulted from a bit signal that should be in the second state but was instead in the first state.

19. (New) The data processing system of Claim 18, wherein the ECC circuitry further comprises:

an address latch coupled to the address input to hold an address of the signal group having an error;

a pattern latch to hold a correction pattern generated by the ECC circuitry of the signal group having an error; and

wherein the address latch and the pattern latch have outputs operable to be accessed in response to an interrupt signaled by the interrupt circuitry.

20. (New) The data processing system of Claim 18, wherein the main memory and the ECC memory are implemented in a technology selected from the group consisting of flash technology and EEPROM technology.

21. (New) The data processing system of Claim 19, further comprising a processor coupled to the non-volatile memory unit's address input, data input and corrected data output, the processor being responsively coupled to the interrupt circuitry; and wherein the processor is operable to respond to an interrupt from the interrupt circuitry by restoring a charge on a failing memory bit location in the main memory or in the ECC memory by writing to the address provided by the address latch.

22. (New) the data processing system of Claim 18, wherein the ECC circuitry further comprises detection circuitry, the detection circuitry operable to determine when a signal group stored in the main memory and in the error signal memory are all logic "1"s.